IN THE CLAIMS

Please amend claim 39 as set forth below.

1. (Previously Presented) An integrated circuit, comprising:

a low resistivity semiconductor substrate having a dielectric region formed therein, a trench defined in the dielectric region and including dielectric sidewalls, and an adjacent cavity defined at least partially by the substrate;

an electroplated conductive material disposed within the trench to produce an inductance having sides and a bottom, the sides of the inductance being bounded by the dielectric sidewalls and the cavity being adjacent the bottom; and

a bottom surface of the semiconductor substrate defining a first recessed region underlying the dielectric region.

2. (Original) The integrated circuit of claim 1, wherein the dielectric region includes a cap layer formed at a top surface of the semiconductor substrate and the cavity extends from the cap layer to a bottom surface of the dielectric region.

3. (Canceled)

4. (Original) The integrated circuit of claim 1, wherein the conductive material includes copper.

5. (Original) The integrated circuit of claim 1, wherein the conductive material is disposed within the trench to a depth of at least five micrometers.

6. (Original) The integrated circuit of claim 1, wherein the dielectric region is formed with a silicon based dielectric.

7. (Original) The integrated circuit of claim 1,

wherein the dielectric region is formed at a top surface of the semiconductor substrate, further comprising an active device formed at the top surface.

8. (Withdrawn) A method of making an integrated circuit, comprising the steps of:

forming a dielectric region in a semiconductor substrate to have a cavity and a trench; and

disposing a conductive material within the trench to produce an inductance.

9. (Withdrawn) The method of claim 8, wherein the step of forming includes the step of forming the dielectric region at a top surface of the semiconductor substrate.

10. (Withdrawn) The method of claim 8, wherein the step of disposing includes the step of plating the conductive material within the trench to form an inductor.

11. (Withdrawn) The method of claim 10, wherein the step of plating includes the step of electroplating copper within the trench.

12. (Withdrawn) The method of claim 10, wherein the step of plating includes the steps of:

applying a plating signal to a bottom surface of the semiconductor substrate; and

coupling the plating signal through the semiconductor substrate to a bottom surface of the trench.

13. (Withdrawn) The method of claim 12, wherein the step of plating includes the step of depositing a barrier material to form a barrier layer at the bottom surface of the trench.

14. (Withdrawn) The method of claim 13, wherein the step of depositing includes the step of depositing a metal selected from the group consisting of platinum, titanium and cobalt along the bottom surface of the trench.

15. (Withdrawn) The method of claim 14, wherein the step of depositing a metal includes the step of forming the barrier layer to include a metal silicide.

16. (Withdrawn) The method of claim 8, further comprising the step of etching a bottom surface of the semiconductor substrate to form a recessed region underlying the dielectric region.

17. (Withdrawn) The method of claim 16, wherein the step of etching includes the step of removing material from the bottom surface of the semiconductor substrate extending to a bottom surface of the trench.

18. (Withdrawn) The method of claim 8, wherein the step of disposing includes the step of disposing the conductive material within the trench to a thickness of at least five micrometers.

19. (Withdrawn)A method of making an integrated circuit, comprising the steps of:

forming a dielectric region in a semiconductor substrate, where the dielectric region has a cavity;

etching the dielectric region to form a trench adjacent to the cavity; and

disposing a conductive material in the trench to form an inductor.

20. (Withdrawn) The method of claim 19, wherein the step of etching includes the step of removing dielectric material to a depth of at least five micrometers from the dielectric region.

21. (Withdrawn) The method of claim 19, wherein the step of disposing includes the step of plating the conductive material within the trench.

22. (Withdrawn) The method of claim 21, wherein the step of plating includes the step of electroplating copper from a bottom surface of the trench to a top surface of the semiconductor substrate.

23. (Withdrawn) The method of claim 19, further comprising the step of depositing a barrier material to form an etch stop on a bottom surface of the trench.

24. (Withdrawn) The method of claim 23, wherein the step of forming includes the step of forming the dielectric region at a top surface of the semiconductor substrate, further comprising the step of etching a second surface of the semiconductor substrate to form a recessed region under the dielectric region.

25. (Withdrawn) The method of claim 24, wherein the step of etching the second surface includes the step of removing material from the second surface extending to the etch stop to form the recessed region.

26. (Withdrawn) The method of claim 25, further comprising the step of mounting the semiconductor substrate to a die attach pad.

27. (Withdrawn) The method of claim 26, wherein the step of mounting includes the step of mounting the recessed region over a pedestal of the die attach pad.

28-33 (Canceled)

34. (Withdrawn) A method of making an integrated circuit, comprising the step of applying a signal to a first surface of a semiconductor substrate to plate an inductor on a second surface of the semiconductor substrate.

35. (Withdrawn) The method of claim 34, wherein the step of applying includes the steps of:

forming a trench on the first surface; and

coupling a plating voltage from the second surface to a bottom of the trench to deposit a conductive material in the trench as the inductor.

36. (Withdrawn) The method of claim 34, further comprising the step of forming a transistor on the second surface of the semiconductor substrate.

37. (Previously Presented) An integrated circuit comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

at least one active component positioned in the active region;

a trench formed in the dielectric region and including side-walls defined by low dielectric constant material; ~~and~~

high conductivity electroplated material in the trench and defining at least a portion of a passive electronic component; and

wherein the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant.

38. (Canceled)

39. (Currently Amended) An integrated circuit ~~as claimed in claim 37~~ comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

at least one active component positioned in the active region;

a trench formed in the dielectric region and including side-walls defined by low dielectric constant material; ~~and~~

high conductivity electroplated material in the trench and defining at least a portion of a passive electronic component; and

wherein the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant, wherein the dielectric material and the array of cavities produce an effective dielectric constant at least ten percent lower than the first dielectric constant.

40. (Previously Presented) An integrated circuit as claimed in claim 39 wherein the effective dielectric constant is approximately 2.5.

41. (Previously Presented) An integrated circuit as claimed in claim 37 wherein the high conductivity electroplated material includes copper.

42. (Previously Presented) An integrated circuit as claimed in claim 37 wherein the trench is elongated and formed in the shape of an inductance.

43. (Previously Presented) An integrated circuit comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

at least one active component positioned in the active region;

a trench formed in the dielectric region and including side-walls defined by low dielectric constant material; ~~and~~

high conductivity electroplated material in the trench and defining at least a portion of a passive electronic component; and

further including a cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity,

electroplated material in the trench.

44. (Previously Presented) An integrated circuit as claimed in claim 43 and further including a die attach pad with a pedestal formed on a surface thereof, the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity.

45. (Previously Presented) An integrated circuit comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

at least one active component positioned in the active region;

an elongated trench formed in the dielectric region and including side-walls defined by low dielectric constant material;

high conductivity material in the trench and defining at least a portion of an inductive component; and

a sealed cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity material in the trench.

46. (Previously Presented) An integrated circuit as claimed in claim 45 wherein the sealed cavity is sealed by a die attach pad with a pedestal formed on a surface thereof, the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity.

47. (Previously Presented) An integrated circuit as claimed in claim 46 wherein the cavity defines a distance between the lower portion of the high conductivity material and the pedestal of approximately one hundred micrometers.

48. (Previously Presented) An integrated circuit as claimed in claim 45 wherein the low dielectric constant material of the side-walls has an effective dielectric constant of approximately 2.5.

49-51 (Canceled)